SGMII and Gb Ethernet PCS

Overview

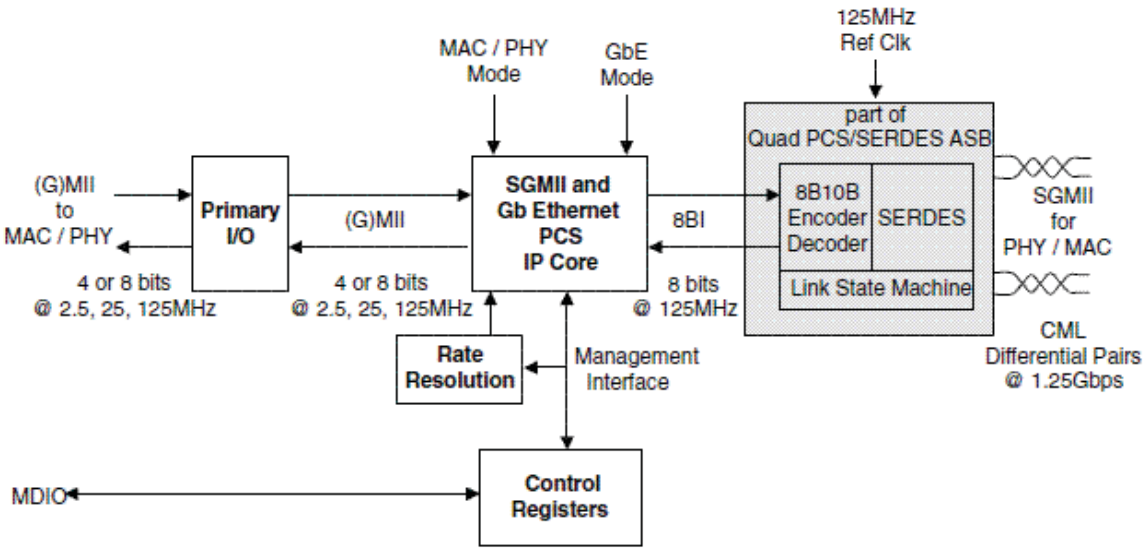
The Lattice **SGMII** and **Gb Ethernet PCS** IP core implements the PCS functions of both the **Cisco SGMII** and the **IEEE 802.3z (1000BaseX)** specifications. The PCS mode is pin selectable. This IP core may be used in bridging applications and/or PHY implementations.

The Serial Gigabit Media Independent Interface (SGMII) is a connection bus for Ethernet Media Access Controllers (MACs) and Physical Layer Devices (PHYs) defined by Cisco Systems. It replaces the classic 22-wire GMII connection with a low pin count, 4-pair, differential SGMII connection. The classic GMII interface defined in the IEEE802.3 specification is strictly for Gigabit rate operation. However, the Cisco SGMII specification defines a method for operating 10 Mbps and 100 Mbps MACs over the interface. Moreover, the Cisco SGMII specification is
comprised of more than just a bus interface definition; it defines a bridging function between SGMII and GMII buses.

These applications can be completely implemented in **LatticeECP3™, LatticeECP2M™ and LatticeSC™** Field Programmable Gate Array (FPGA) devices. As an example, Lattice has developed a reference design for a complete SGMII-to-(G)MII bridge. This reference design is included with the SGMII and Gb Ethernet PCS IP Core package and is described in detail in Appendix C.

The core can be instantiated, synthesized and simulated through **IPexpress™** software.

Application



Key Features

- Implements PCS functions of the Cisco SGMII Specification, Revision 1.7
- Implements PCS functions for IEEE 802.3z (1000BaseX)
- Dynamically selects SGMII/1000BaseX PCS operation
- Supports MAC or PHY mode for SGMII auto-negotiation
- Supports (G)MII data rates of 1Gbps, 100Mbps, 10Mbps
- Provides Management Interface Port for control and maintenance
- Includes Easy Connect option for seamless integration with Lattice's Tri-Speed MAC (TSMAC) IP core

Resource Utilization

LatticeECP3[1]

Configuration				SLICEs	LUTs	REGs	EBRs	f_{MAX}[2] (MHz)
GMII Style	RX CTC Mode	FIFO Low Threshold	FIFO High Threshold					
Classic	None	-	-	749	877	898	0	125
Classic	Static	16	32	835	999	1007	1	125
Easy Connect	Static	240	260	704	848	851	1	125
Easy Connect	Dynamic	-	-	729	864	882	1	125

1. Performance and utilization data are generated targeting an LFE3-70EA-7FN484CES device using Lattice Diamond 1.1 and Synplify Pro D-2010.03L-SP1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.
2. The SGMII requires operation at 125 MHz, therefore a higher frequency is not stated. However this core can easily attain frequencies above 140 MHz in a LatticeECP3 speed grade 7 device.

LatticeECP2M[1]

Configuration				SLICEs	LUTs	REGs	EBRs	f_{MAX}[2] (MHz)
GMII Style	RX CTC Mode	FIFO Low Threshold	FIFO High Threshold					
Classic	None	-	-	750	878	898	0	125
Classic	Static	16	32	838	1001	1007	1	125
Easy Connect	Static	240	260	709	850	851	1	125
Easy Connect	Dynamic	-	-	727	862	860	1	125

1. Performance and utilization data are generated targeting an LFE2M35E-6F672C device using Lattice Diamond 1.1 and Synplify Pro D-D-2010.03L-SP1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family.
2. The SGMII requires operation at 125 MHz, therefore a higher frequency is not stated. However this core can easily attain frequencies above 140 MHz in a LatticeECP2M speed grade 6 device.

LatticeSC/M[1]

Configuration				SLICEs	LUTs	REGs	EBRs	f_{MAX}[2] (MHz)
GMII Style	RX CTC Mode	FIFO Low Threshold	FIFO High Threshold					
Classic	None	-	-	753	952	913	0	125
Classic	Static	16	32	730	922	886	1	125
Easy Connect	Static	240	260	608	781	730	1	125
Easy Connect	Dynamic	-	-	741	957	875	1	125

1. Performance and utilization data are generated targeting an LFSC3GA25E-6FFA1020C device using Lattice Diamond 1.1 and Synplify Pro D-2010.03L-SP1 software. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC/M family.
2. The SGMII requires operation at 125 MHz, therefore a higher frequency is not stated. However this core can easily attain frequencies above 200 MHz in a LatticeSC speed grade 6 device.

Ordering Information

LatticeECP3	GBE-SGMII-E3-U1
LatticeECP2M	GBE-SGMII-PM-U1
LatticeSC	GBE-SGMII-SC-U1

IP Version: 3.4

Evaluate: To download a full evaluation version of this IP, please go to the Lattice IP Server tab in the IPexpress Main Window. All LatticeCORE IP that are available for download wil be visible on this tab.
Purchase: To find out how to purchase this IP Core, please contact your **local Lattice Sales Office**.