

STF18N60DM2

N-channel 600 V, 0.260 Ω typ., 13 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet - production data

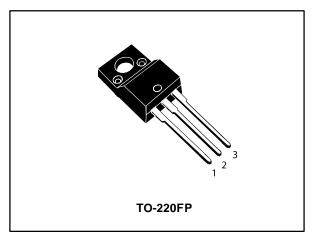
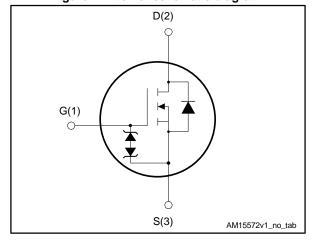


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} R _{DS(on)} max.		ID
STF18N60DM2	600 V	0.295 Ω	13 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh $^{\text{TM}}$ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF18N60DM2	18N60DM2	TO-220FP	Tube

Contents STF18N60DM2

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STF18N60DM2 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vgs	Gate-source voltage	±25	V
I _D ⁽¹⁾	Drain current (continuous) at T _{case} = 25 °C	13	Λ.
ID(*/	Drain current (continuous) at T _{case} = 100 °C	7.6	Α
I _{DM} ⁽²⁾	Drain current (pulsed) 48		Α
Ртот	Total dissipation at T _{case} = 25 °C 25		W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	40	V/ns
dv/dt ⁽⁴⁾	MOSFET dv/dt ruggedness	50	V/IIS
Viso	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T _{stg}	Storage temperature range -55 to 150		°C
Tj	Operating junction temperature range	-55 (0 150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	5	°C // //
R _{thj-amb}	Thermal resistance junction-ambient 62.5		°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR} ⁽¹⁾	Avalanche current, repetitive or not repetitive	2.5	Α
E _{AR} ⁽²⁾	Single pulse avalanche energy		mJ

Notes:

⁽¹⁾ Limited by maximum junction temperature.

⁽²⁾ Pulse width is limited by safe operating area.

 $^{^{(3)}}$ I_{SD} \leq 12 A, di/dt \leq 400 A/ μ s, V_{DS}(peak) < V(BR)DSS, V_{DD} = 80% V(BR)DSS.

 $^{^{(4)}}$ V_{DS} ≤ 480 V.

 $^{^{(1)}}$ Pulse width is limited by T_{jmax} .

 $^{^{(2)}}$ starting T_j = 25 °C, I_D = $I_{AR},\,V_{DD}$ = 50 V.

Electrical characteristics STF18N60DM2

2 Electrical characteristics

(T_{case}= 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			٧
	Zoro goto voltago droin	$V_{GS} = 0 \text{ V}, V_{DS} = 600 \text{ V}$			1.5	
IDSS	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V, T _{case} = 125 °C			100	μΑ
Igss	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on- resistance	V _G S = 10 V, I _D = 6 A		0.260	0.295	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	800	ı	
Coss	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz},$	-	40	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	1.33	-	ρ.
Coss eq. (1)	Equivalent output capacitance	, , ,		80	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	5.6	-	Ω
Qg	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 12 \text{ A},$	-	20	•	
Q _{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge	-	5.2	-	nC
Q_{gd}	Gate-drain charge	behavior")	-	8.5	-	

Notes:

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Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 300 \text{ V}, I_D = 6 \text{ A R}_G = 4.7 \Omega,$	ı	13.5	ı	
tr	Rise time	V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching		8	-	
$t_{d(off)}$	Turn-off-delay time	times" and Figure 19: "Switching	-	9.5	-	ns
t _f	Fall time	time waveform")	-	32.5	-	

 $^{^{(1)}}$ Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when VDS increases from 0 to 80% VDSS

Table 8: Source-drain diode

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		12	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		48	А
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 12 A	-		1.6	V
t _{rr}	Reverse recovery time	$I_{SD} = 12 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	125		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V (see Figure 16: "Test circuit for inductive load	-	675		nC
I _{RRM}	Reverse recovery current	switching and diode recovery times")	ı	11		А
t _{rr}	Reverse recovery time	$I_{SD} = 12 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s,}$	-	190		ns
Qrr	Reverse recovery charge	V_{DD} = 60 V, T_j = 150 °C (see Figure 16: "Test circuit for	-	1200		nC
I _{RRM}	Reverse recovery current	inductive load switching and diode recovery times")	-	13		А

Notes:

 $^{^{(1)}}$ Pulse width is limited by safe operating area.

 $^{^{(2)}\}text{Pulse}$ test: pulse duration = 300 $\mu\text{s},$ duty cycle 1.5%.

2.1 Electrical characteristics (curves)

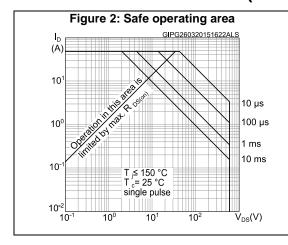


Figure 3: Thermal impedance $K = \frac{GC20940}{\delta = 0.5}$ $\frac{\delta = 0.2}{\delta = 0.02}$ $\frac{\delta = 0.02}{\delta = 0.01}$ $\frac{\delta = 0.02}{\delta = 0.01}$ $\frac{\delta = 0.02}{\delta = 0.02}$ $\frac{\delta = 0.02}{\delta = 0.01}$ $\frac{\zeta_{lh} = K^*R_{lh}_{lh}_{lh}_{lh}}{\delta = t_{lh}/T}$ $\frac{10^{-3}}{10^{-4}}$ $\frac{10^{-3}}{10^{-4}}$

Figure 4: Output characteristics

ID GIPG290415FQ6GOCH

(A) V_{GS} = 7,8,9,10 V

24

20

16

12

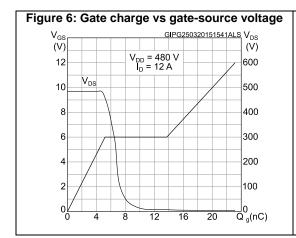
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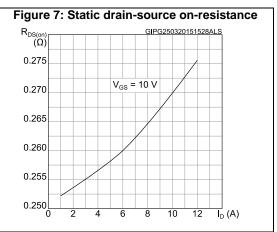
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0

0

2 4 6 8 10 12 V_{DS} (V)





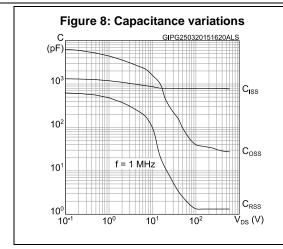


Figure 10: Normalized on-resistance vs temperature

R_{DS(on)} GIPG250320151534ALS

(norm.)

2.2

V_{GS}= 10 V

1.8

1.4

1.0

0.6

0.2

-75

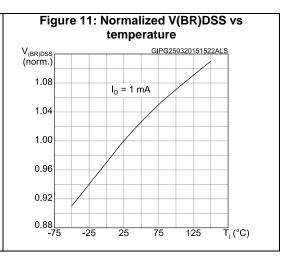
-25

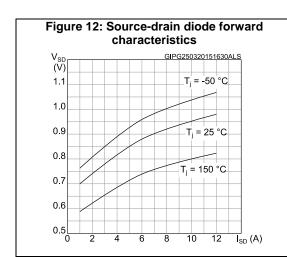
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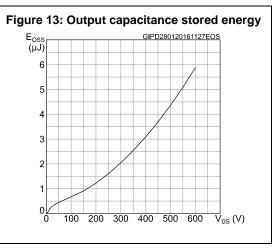
75

125

T_j (°C)







Test circuits STF18N60DM2

3 Test circuits

Figure 14: Test circuit for resistive load switching times

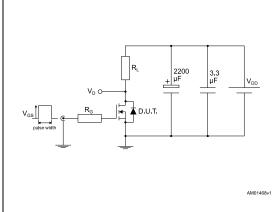


Figure 15: Test circuit for gate charge behavior

12 V 47 KΩ 100 Ω 1 KΩ

Vos 1 100 Ω 1 LΩ

2200 1 1 KΩ

AM01469-1

Figure 16: Test circuit for inductive load switching and diode recovery times

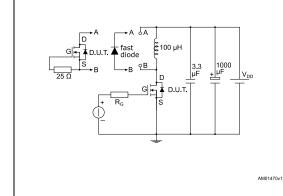


Figure 17: Unclamped inductive load test circuit

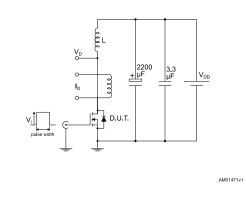


Figure 18: Unclamped inductive waveform

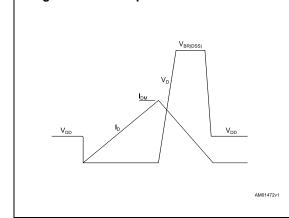
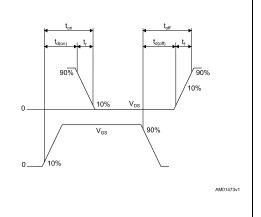


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



4.1 TO-220FP package information

Figure 20: TO-220FP package outline

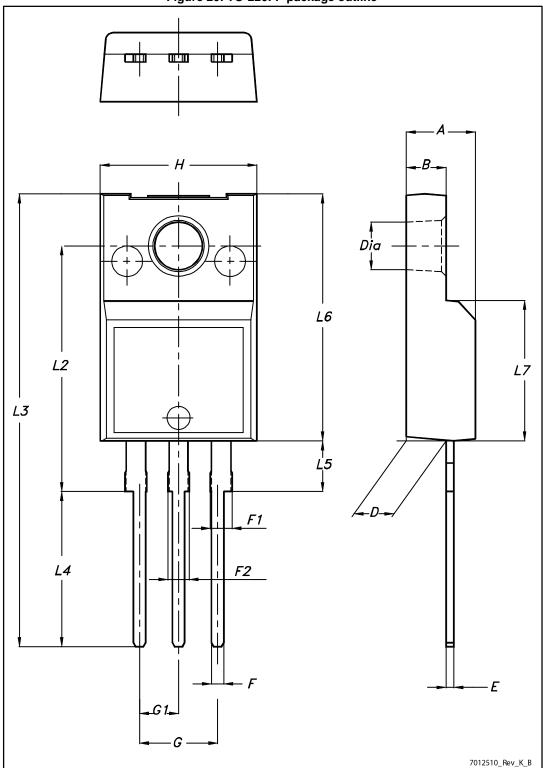


Table 9: TO-220FP package mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
Α	4.4		4.6
В	2.5		2.7
D	2.5		2.75
Е	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
Н	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history STF18N60DM2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
01-Apr-2015	1	First release.
21-May-2015	2	Text edits throughout document In Section 2.1 Electrical characteristics (curves): - updated Figure 4: Output characteristics - updated Figure 5: Transfer characteristics
02-Jul-2015	3	Updated title and I _D values in features and Table 1
28-Jan-2016	4	Updated Section 2.1: "Electrical characteristics (curves)".

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