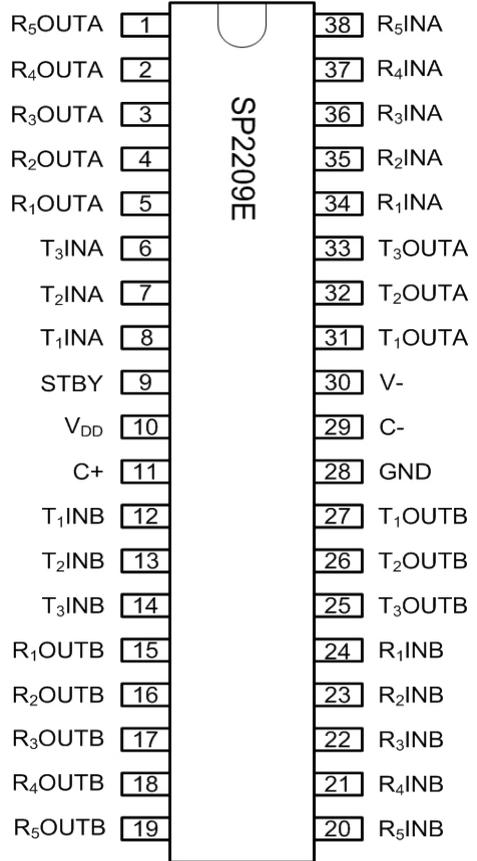




High ESD Dual Port RS-232 Transceiver

FEATURES

- Meets True EIA/TIA-232-F Standards
- Complies with 89/336/EEC EMC Directive
- Single +12V Power Supply
- <5mA Low Power CMOS Operation
- 100µA Low Standby Current
- Operates With +3V or +5V Logic
- Provides +3.3V to +5V Standby Supply
- Two Complete Serial Ports, 6 Drivers And 10 Receivers
- One Receiver On Each Port Active In Standby
- Failsafe Receiver Outputs
- 460kbps Minimum Data Rate
- Ideal For High Speed RS-232 Applications
- Low EMI Emissions (EN55022)
- Pin Compatible To ADM2209E device
- Enhanced ESD Specifications:
 - +15kV Human Body Model
 - +15kV IEC61000-4-2 Air Discharge
 - +8kV IEC61000-4-2 Contact Discharge
- Fast Transient Burst (EFT) Immunity (IEC61000-4-4)



Now Available in Lead Free Packaging

DESCRIPTION

The rugged, high ESD **SP2209E** device is a complete dual RS-232 port integrated onto a single integrated circuit. Six drivers and ten receivers provide designers a dual port solution fully meeting the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in applications such as personal desktop computers and workstations. Features include high transmission rates, low power consumption, an internal charge-pump power supply that requires only two capacitors, space saving 38-pin TSSOP package dimensions, and compatibility with the EU directive on electromagnetic compatibility. This device is ideal for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged. This device is also immune to high RF field strengths without special shielding precautions.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{DD}-0.3V to +14.0V
 V_{STBY}-0.3V to +7.0V

Input Voltages

TxINA.....-0.3V to ($V_{STBY} + 0.3V$)
 TxINB.....-0.3V to ($V_{STBY} + 0.3V$)
 RxINA.....+15V
 RxINB.....+15V

Output Voltages

TxOUTA.....±15V
 TxOUTB.....±15V
 RxOUTA,-0.3V to ($V_{STBY} + 0.3V$)
 RxOUTB,-0.3V to ($V_{STBY} + 0.3V$)

Short-Circuit Duration

TxOUTA.....Continuous
 TxOUTB.....Continuous

Storage Temperature.....-65°C to +150°C

Power Dissipation per package

38-pin TSSOP (derate 914.3mW/°C above +70°C).....1200mW

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{DD} = +12.0V \pm 10\%$, $V_{STBY} = +3.3V \pm 5\%$ or $+5V \pm 10\%$, $C1 = C2 = 0.1\mu F$, and $T_{AMB} = T_{MIN}$ to T_{MAX} .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current			5	mA	no load, all driver inputs at 0.4V or 2.1V, All receiver inputs at +15V or -15V
Standby Supply Current, V_{STBY}		100	200	µA	no load, All driver inputs at V_{STBY} or open
CMOS LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.4	V	$T_{AMB} = 25^\circ C$
Input Logic Threshold HIGH	2.1			V	$T_{AMB} = 25^\circ C$
Input Leakage Current		10	25	µA	Driver input at 0V
Output Voltage LOW		0.2	0.4	V	$I_{OL} = +1.6mA$
Output Voltage HIGH	2.4			V	$I_{OH} = -40\mu A$
Output Leakage Current		+/-0.05	+/-5	µA	V _{DD} = 0V, (except R ₅ OUTA and R ₅ OUTB)
DRIVER OUTPUTS					
Output Voltage Swing	+/-5.0	+/-9.0		V	all driver outputs loaded with 3kΩ to GND
Output Resistance	300			Ω	$V_{DD} = V_{STBY} = 0V$, $V_{OUT} = \pm 2V$
Output Short-Circuit Current	+/-5	+/-15	+/-30	mA	one driver output shorted, $V_{IN} = 0.8V$, $V_{OUT} = 0V$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the following specifications apply for $V_{DD} = +12.0V \pm 10\%$, $V_{STBY} = +3.3V \pm 5\%$ or $+5V \pm 10\%$, $C1 = C2 = 0.1\mu F$, and $T_{AMB} = T_{MIN}$ to T_{MAX} .

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.4	1.45		V	
Input Threshold HIGH		1.7	2.4	V	
Input Hysteresis		0.25		V	
Input Resistance	3	5	7	k Ω	$V_{IN} = \pm 15V$
TIMING CHARACTERISTICS					
Driver Maximum Data Rate	460			kbps	$R_L = 3k\Omega$ to $7k\Omega$, $C_L = 50pF$ to $470pF$
Driver Maximum Data Rate	460			kbps	$R_L = 3k\Omega$ to $7k\Omega$, $C_L = 50pF$ to $1000pF$, $T_{AMB} = 0^\circ C$ to $+85^\circ C$, $V_{STBY} = 5V \pm 10\%$ only
Driver Maximum Data Rate	920			kbps	$R_L = 3k\Omega$ to $7k\Omega$, $C_L = 50pF$ to $470pF$, $V_{STBY} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$
Driver Propagation Delay, t_{PHL}		1.0		μs	$R_L = 3k\Omega$, $C_L = 1000pF$, refer to Figures 3 and 5
Driver Propagation Delay, t_{PLH}		1.0		μs	$R_L = 3k\Omega$, $C_L = 1000pF$, refer to Figures 3 and 5
Driver Transition-Region Slew Rate	6	16		V/ μs	$R_L = 3k\Omega$ to $7k\Omega$, $C_L = 50pF$ to $470pF$, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$
Driver Transition-Region Slew Rate	4	16		V/ μs	$R_L = 3k\Omega$ to $7k\Omega$, $C_L = 50pF$ to $1000pF$, $V_{STBY} = 5V \pm 10\%$ only, measurements taken from $-3.0V$ to $+3.0V$ or $+3.0V$ to $-3.0V$
Receiver Maximum Data Rate	460			kbps	$C_L = 150pF$
Receiver Maximum Data Rate	920			kbps	$C_L = 150pF$, $V_{STBY} = 5V \pm 5\%$ only
Receiver Propagation Delay, t_{PHL} (R1x - R4x)		0.4	0.75	μs	$C_L = 150pF$, refer to Figures 4 and 6
Receiver Propagation Delay, t_{PLH} (R1x - R4x)		0.4	0.75	μs	$C_L = 150pF$, refer to Figures 4 and 6
Receiver Propagation Delay, t_{PHL} (R5x)		1.0	2.0	μs	$C_L = 150pF$, refer to Figures 4 and 6
Receiver Propagation Delay, t_{PLH} (R5x)		1.0	2.0	μs	$C_L = 150pF$, refer to Figures 4 and 6
Receiver Output Rise Time		30		ns	refer to Figures 4 and 6
Receiver Output Fall Time		30		ns	refer to Figures 4 and 6
OPERATING CHARACTERISTICS					
Operating voltage Range, V_{DD}	+10.8	+12.0	+13.2	V	
Standby Voltage Range, V_{STBY}	+3.15		+5.5	V	
Operating Temperature, T_{AMB}	-40		+85	$^\circ C$	

NAME	FUNCTION	Pin Number
R ₅ OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A	1
R ₄ OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A	2
R ₃ OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A	3
R ₂ OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A	4
R ₁ OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A	5
T ₃ INA	+3.3V to +5V TTL/CMOS logic level driver input for port A	6
T ₂ INA	+3.3V to +5V TTL/CMOS logic level driver input for port A	7
T ₁ INA	+3.3V to +5V TTL/CMOS logic level driver input for port A	8
STBY	+3.3V to +5V standby power supply for receivers R ₅ OUTA and R ₅ OUTB	9
V _{DD}	+12V Power Supply	10
C+	Positive terminal for the polarized C1 charge pump capacitor	11
T ₁ INB	+3.3V to +5V TTL/CMOS logic level driver input for port B	12
T ₂ INB	+3.3V to +5V TTL/CMOS logic level driver input for port B	13
T ₃ INB	+3.3V to +5V TTL/CMOS logic level driver input for port B	14
R ₁ OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B	15
R ₂ OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B	16
R ₃ OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B	17
R ₄ OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B	18
R ₅ OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B	19
R ₅ INB	RS-232 receiver input for port B	20
R ₄ INB	RS-232 receiver input for port B	21
R ₃ INB	RS-232 receiver input for port B	22
R ₂ INB	RS-232 receiver input for port B	23
R ₁ INB	RS-232 receiver input for port B	24
T ₁ OUTB	RS-232 driver output for port B	25
T ₂ OUTB	RS-232 driver output for port B	26
T ₃ OUTB	RS-232 driver output for port B	27
GND	Ground	28
C-	Negative terminal for the polarized C1 charge pump capacitor	29
V ₋	-12V output generated by the charge pump at the negative terminal of the polarized C2 charge pump capacitor	30
T ₁ OUTA	RS-232 driver output for port A	31
T ₂ OUTA	RS-232 driver output for port A	32
T ₃ OUTA	RS-232 driver output for port A	33
R ₁ INA	RS-232 receiver input for port A	34
R ₂ INA	RS-232 receiver input for port A	35
R ₃ INA	RS-232 receiver input for port A	36
R ₄ INA	RS-232 receiver input for port A	37
R ₅ INA	RS-232 receiver input for port A	38

Table 1. Device Pin Description

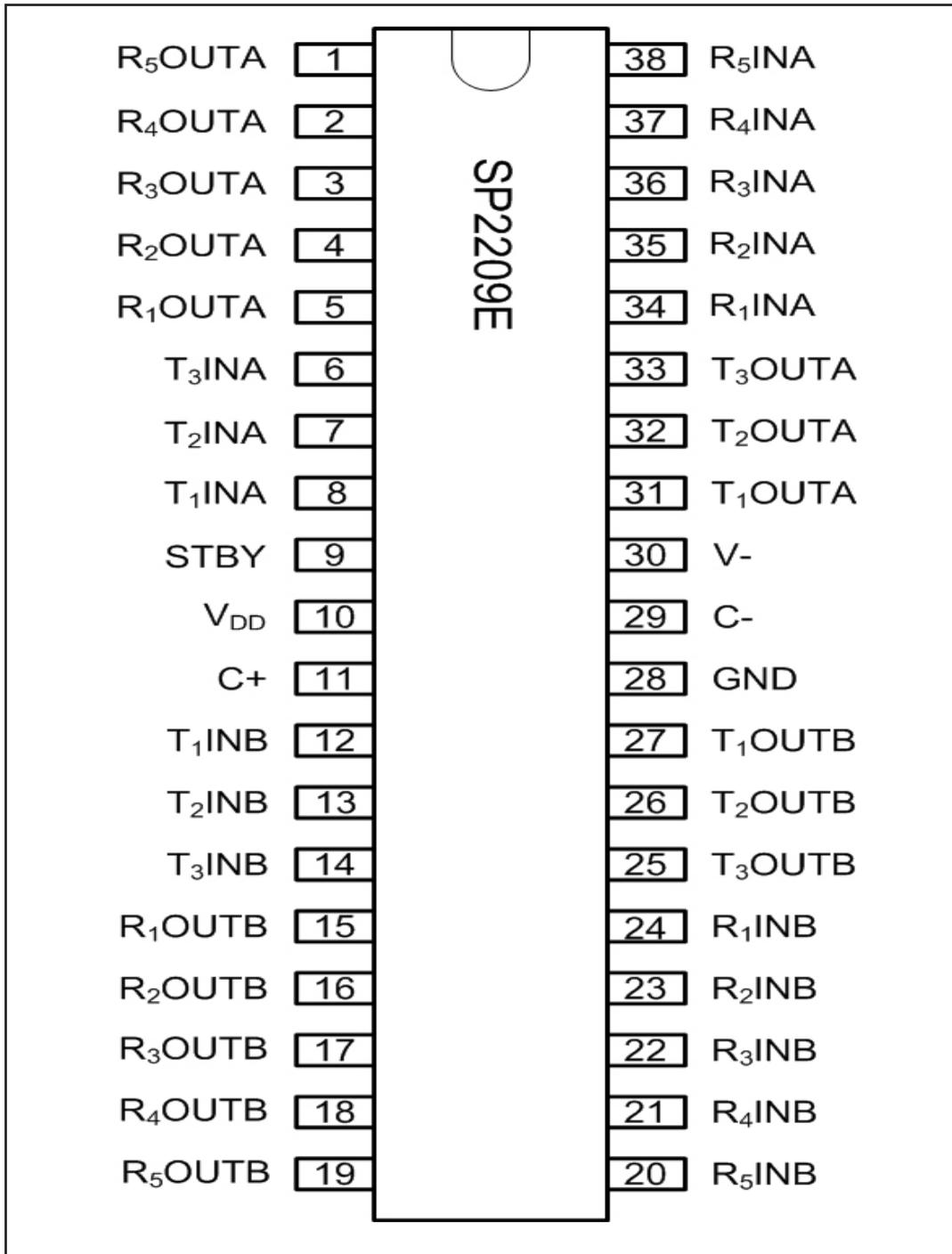


Figure 1. Pinout Configuration for the SP2209E

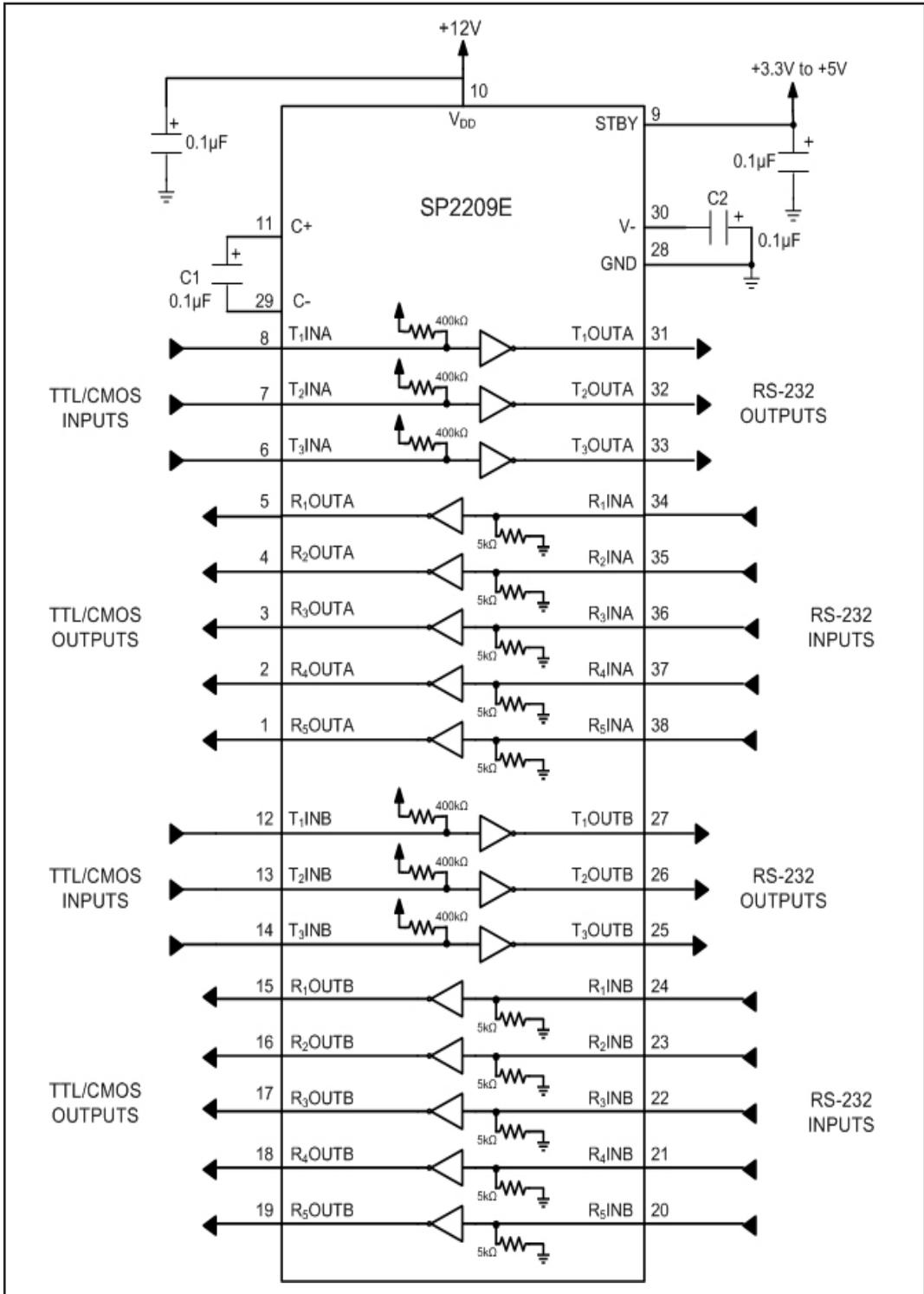


Figure 2. SP2209E Typical Operating Circuits

The **SP2209E** device is a rugged, high ESD, complete dual RS-232 port integrated onto a single integrated circuit. Six drivers and ten receivers provide a dual port solution fully meeting the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in applications such as personal desktop computers and workstations. Refer to Figure 2 for a typical operating circuit.

Features include high transmission rates, low power consumption, space saving package dimensions, and compatibility with the EU directive on electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference including high levels of electrostatic discharge. This device is ideal for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged. This device is also immune to high RF field strengths without special shielding precautions. Emissions are also controlled to within very strict limits.

The **SP2209E** device features the inverter portion of Exar's proprietary and patented (U.S. 5,306,954) on-board charge pump circuitry that generates a -9V voltage level from a single +12V power supply. The SP2209E device can operate at data rates up to 460kbps fully loaded.

Its low power CMOS operation makes the **SP2209E** device an ideal choice for power sensitive designs. The **SP2209E** device has two receivers, one for each RS-232 port, that remains active in the standby mode to allow the monitoring of peripheral devices while the rest of the system is in a power-saving standby mode. This allows the **SP2209E** device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100mA.

THEORY OF OPERATION

The **SP2209E** device is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. The Exar proprietary charge pump
4. Standby circuitry

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to EIA/TIA-232 levels with an inverted sense relative to the input logic levels. With $V_{DD} = +12V$, the typical RS-232 output voltage swing is $\pm 9V$ with no load and $\pm 5V$ minimum fully loaded. Unused driver input may be left unconnected with an internal pull-up resistor pulling the inputs high forcing the driver outputs into a low state. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA/TIA-232F and all other previous versions.

The drivers typically operate at a minimum data rate of 460kbps fully loaded with 3k Ω in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. The **SP2209E** device is ideal for the new generation modem standards which require data rates greater than 460kbps. Refer to Figures 3 and 5 for driver propagation delay test circuit and waveforms, respectively.

Receivers

The Receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. Should an input be left unconnected, an internal 5k Ω pulldown resistor to ground will commit the output of the receiver to a HIGH state. Receiver inputs are protected against over-voltages of up to $\pm 15V$. Refer to Figures 4 and 6 for receiver propagation delay test circuits and waveforms, respectively.

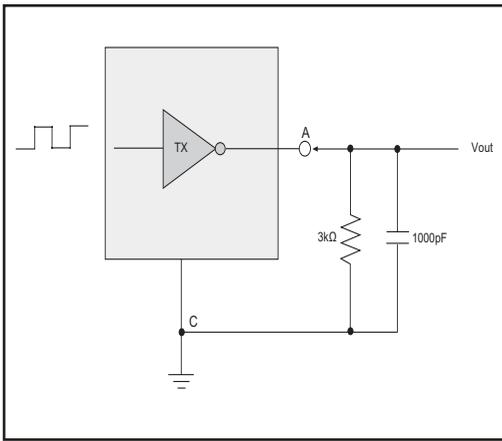


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

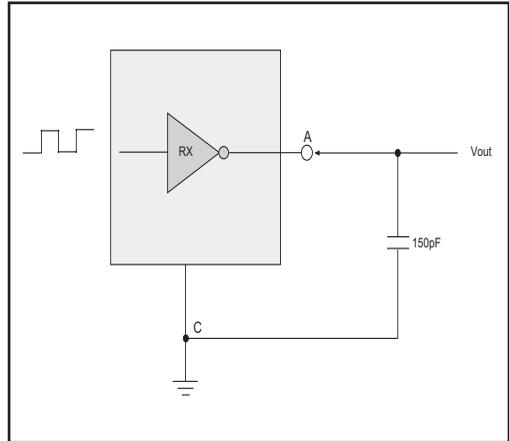


Figure 4 Receiver Propagation Delay and Transition Time Test Circuit

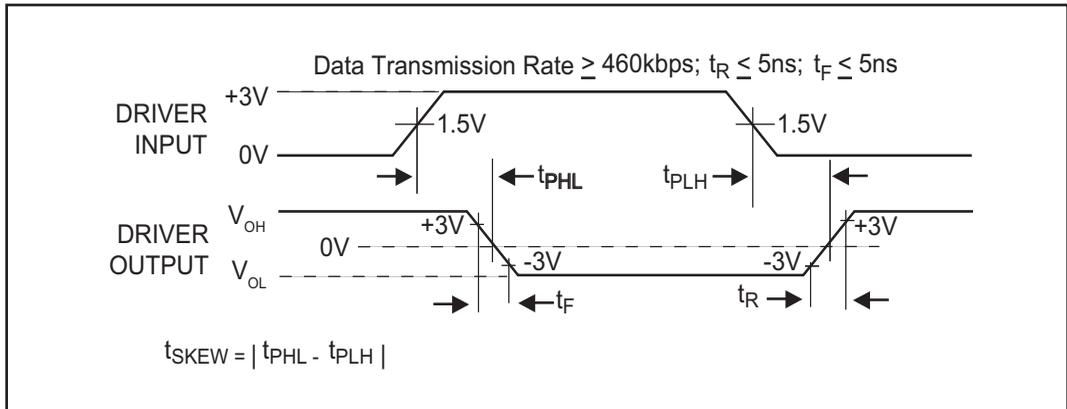


Figure 5. Driver Propagation Delay

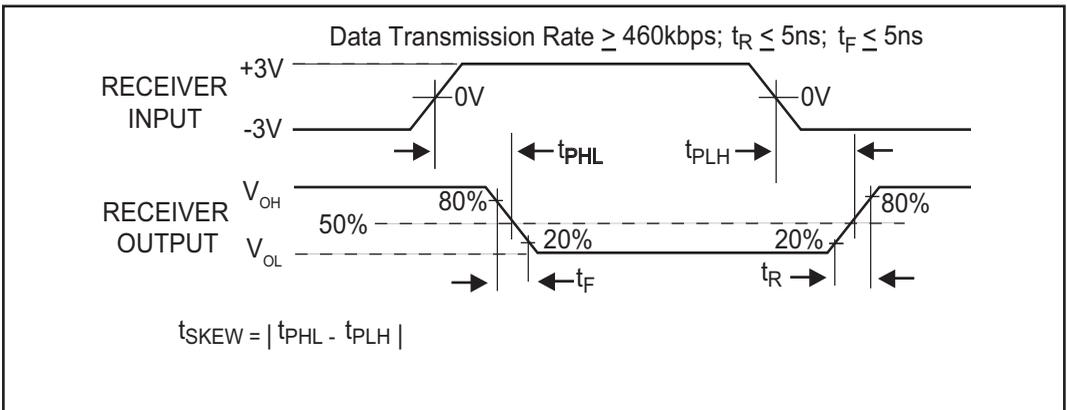


Figure 6. Receiver Propagation Delay

One receiver in each RS-232 port can be kept active by a low current, +3.3V to +5V power supply while the rest of the channels are powered down. This allows the **SP2209E** device to monitor peripheral devices while the rest of the system is in a power-saving standby mode. The **SP2209E** device can be implemented as a power management device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100 μ A.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines and inputs with slow transition times.

Charge Pump

The charge pump is an Exar-patented design (U.S. 5,306,954) and uses a unique approach compared to older less-efficient designs. The charge pump requires two external capacitors using a two-phase voltage shifting technique with a 200kHz internal oscillator to attain a -9V power supply. Refer to Figure 7 for the internal charge pump circuit. The internal power supply consists of a charge pump that provides output voltages of at least +/-5V regardless of the input voltage (V_{DD}). This is important to maintain compliant RS-232 levels regardless of power supply fluctuations. A description of each phase follows.

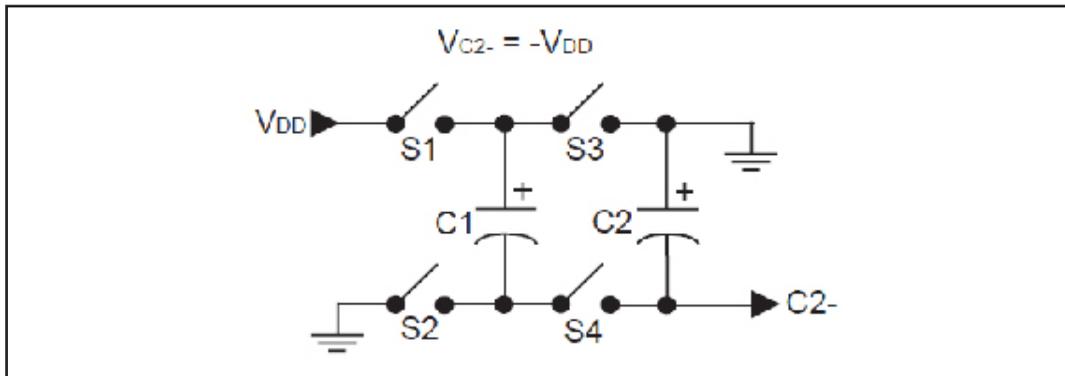


Figure 7. Charge Pump Circuit

Phase 1

— V_{DD} charge storage — S1 and S2 are closed. S3 and S4 are open. During this phase of the clock cycle, the positive side of C_1 is connected to GND. The negative side of capacitor C_2 is now 2 times V_{CC} .

Phase 2

— V_{DD} transfer — S1 and S2 are closed. S3 and S4 are open. The negative side of capacitor C_2 is connected to C_2^- . The positive side of C_2 is connected to GND. This transfers a negative generated voltage to C_2^- . A negative voltage is built up on the negative side of C_2 with each cycle of the oscillator. If the current drawn is small, the output voltage at C_2^- will be close to $-V_{DD}$. As the current drawn from C_2^- increases, the output voltage will decrease with magnitude. The charge pump cycle will continue as long as the operational conditions for the internal oscillator present. Refer to Figure 8 for the internal charge pump waveforms.

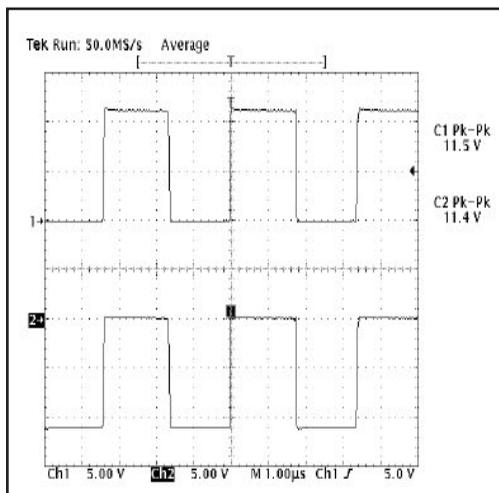


Figure 8. Charge Pump Waveforms

Standby Circuitry

The **SP2209E** device incorporates power saving, on board standby circuitry. The standby current is typically less than $100\mu\text{A}$. The **SP2209E** device automatically enters a standby mode when the V_{DD} power supply is removed. An internal comparator generates an internal shutdown signal that disables the external oscillator disengaging the charge pump. Refer to Figure 9 for the internal standby detection circuit.

The inverted output V- goes to ground. All driver outputs are disabled. The inputs for receivers 1 through 4 for both ports A and B are at high impedance. Receiver 5 for both ports A and B remain fully active as power management receiver lines to system peripherals that may come online during the standby mode.

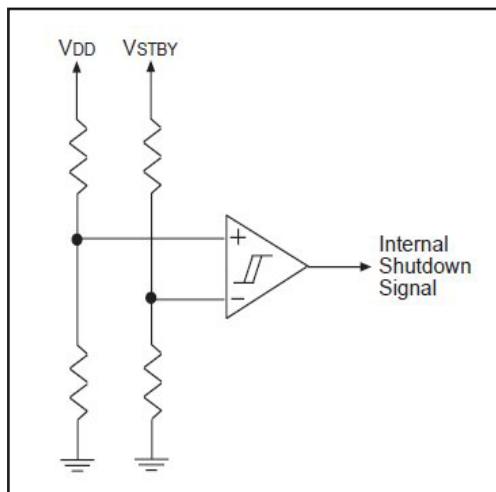


Figure 9 Internal Standby Detection Circuit

ESD TOLERANCE

The **SP2209E** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least $\pm 15\text{kV}$ without damage nor latch-up.

There are different methods of ESD testing applied:

- a) MIL-STD-883, Method 3015.7
- b) IEC 61000-4-2 Air-Discharge
- c) IEC 61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semi-conductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in Figure 10. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the IC's tend to be handled frequently.

The IEC-61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC

61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC 61000-4-2 is shown on Figure 11. There are two methods within IEC 61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the

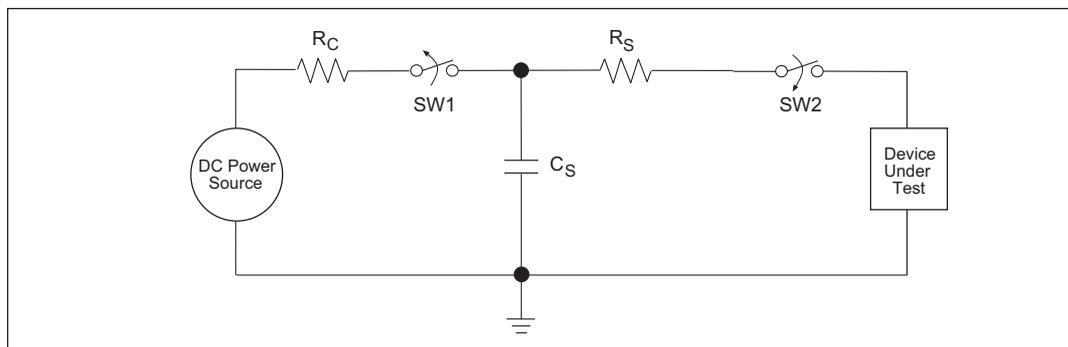


Figure 10. ESD Test Circuit for Human Body Model

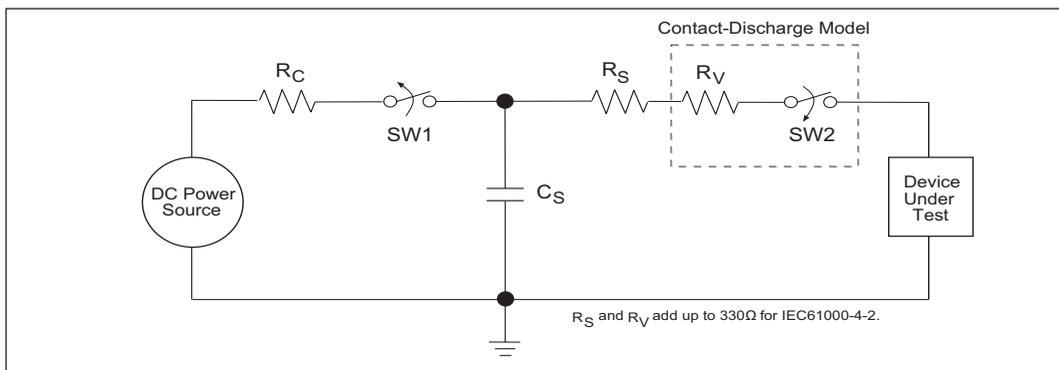


Figure 11. ESD Test Circuit for IEC61000-4-2

equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in Figures 10 and 11 represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S , the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively. For IEC-61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω and 150pF, respectively.

The higher C_S value and lower R_S value in the IEC61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

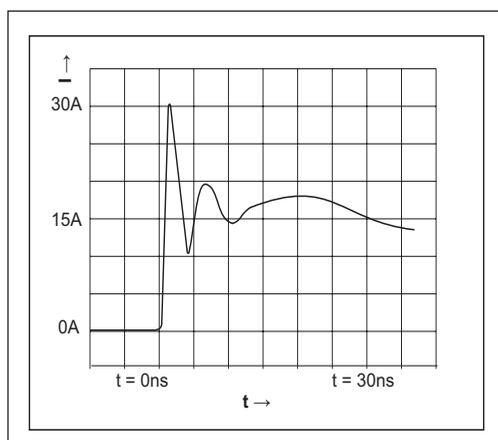


Figure 12. ESD Test Waveform for IEC61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC61000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 2. Transceiver ESD Tolerance Levels

APPLICATIONS

With six drivers and ten receivers, the **SP2209E** device is ideal for applications requiring two RS-232 ports such as in desktop or portable computers. Refer to Figure 13. For typical DB9 serial ports for Data Terminal Equipment (DTE) to Data Circuit Terminating Equipment (DCE) interface implementation, 2 data lines, TxD and RxD, and 6 control lines, RTS, DTR, DSR, CTS, and RI, are required. The straight-through pinout for data lines in the **SP2209E** device allows a simplified PCB layout allowing ground lines to separate the signal lines and ground planes to be placed beneath the IC without the complication of a multi-layer PCB layout.

A receiver from each port, R5INA and R5INB, are active while the rest of the channels are powered down. This allows the **SP2209E** device to monitor peripheral devices while the rest of the system is in a power-saving standby mode. Failsafe receiver outputs are pulled high if the receiver inputs are left unconnected or at zero input. The **SP2209E** device can be implemented as a power management device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100 μ A.

A standard serial mouse can be powered from the **SP2209E** drivers. Two driver outputs connected in parallel and set to V_{OH} can be used to supply power to the V+ pin of the mouse. The third driver is set to V_{OL} to sink current from the V- terminal. Typical mouse specifications are 10mA at +6V and 5mA at -6V.

LapLink Compatibility

The **SP2209E** can operate up to 460kbps data under maximum driveload conditions of $C_L = 1000\text{pF}$ and $R_L = 3\text{k}\Omega$ at minimum power supply voltages.

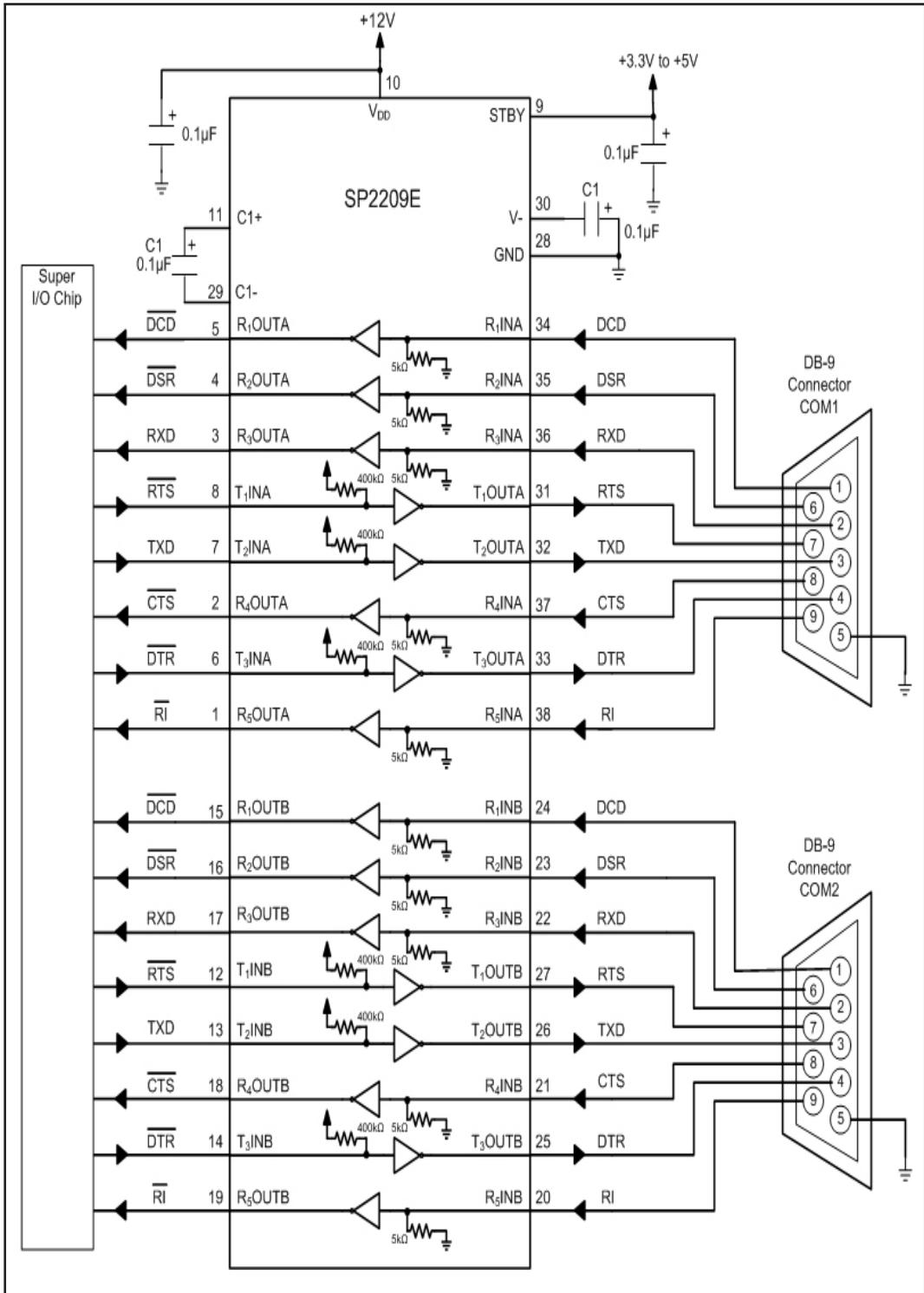
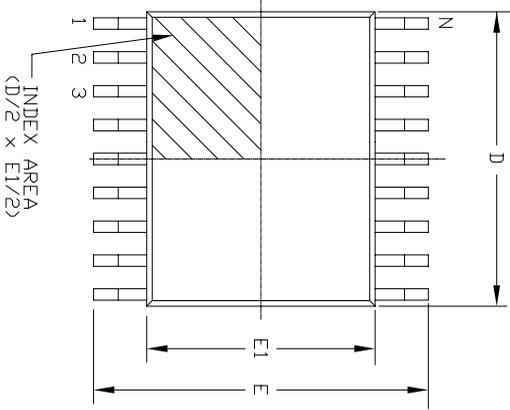


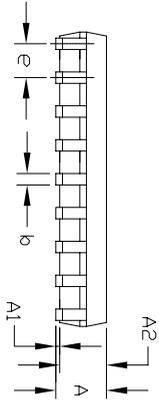
Figure 13. Dual Serial Port Application with Two DB-9 Connectors

PACKAGE: 38 PIN TSSOP

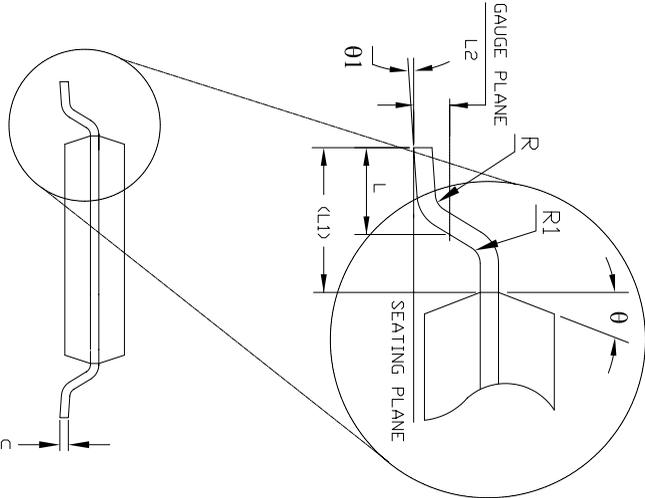
Top View



Side View



Front View



REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATOR	04/19/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

38 Pin TSSOP JEDEC MO-153 Variation BD-1							
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)			MAX
	MIN	NOM	MAX	MIN	NOM	MAX	
A	—	—	1.20	—	—	—	0.047
A1	0.05	—	0.15	0.002	—	—	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041	—
b	0.17	—	0.27	0.007	—	0.011	—
c	0.09	—	0.20	0.004	—	0.008	—
E	6.40 BSC			0.252 BSC			—
E1	4.30	4.40	4.50	0.169	0.173	0.177	—
e	0.50 BSC			0.020 BSC			—
L	0.45	0.60	0.75	0.018	0.024	0.030	—
L1	1.00 REF			0.039 REF			—
L2	0.25 BSC			0.010 BSC			—
R	0.09	—	—	0.035	—	—	—
R1	0.09	—	—	0.035	—	—	—
theta	12° REF			12° REF			—
theta1	0°	—	8°	0°	—	8°	—
D	9.60	9.70	9.80	0.378	0.382	0.386	—
N	38			38			—

		EXAR CORPORATION	
		38 PIN TSSOP PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 38-PIN TSSOP	
By: JL	Date: 11/28/07	Revision: B	Sheet: 1 OF 1

ORDERING INFORMATION

Part Number	Temp. Range	Package
SP2209EEY-L	-40°C to +85°C	38 Pin TSSOP
SP2209EEY-L/TR	-40°C to +85°C	38 Pin TSSOP

Note: "/TR" is for tape and Reel option. "-L" is for lead free packaging

REVISION HISTORY

DATE	REVISION	DESCRIPTION
2006	--	Legacy Sipex Datasheet
07/16/12	1.0.0	Convert to Exar Format and update ordering information. Change ESD specifications to IEC61000-4-2

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